**8 /10/12位低功耗、高性能、带有缓冲的8通道DAC**

## 1. Description

- The uDAC8X08/uDAC8X10/uDAC8X12 is a full-featured, general-purpose OCTAL 8-/10-12-bit voltage-output digital-to-analog converter (DAC) that can operate from a single 2.7-V to 5.5-V supply and consumes 1.95 mW at 3 V and 4.85 mW at 5 V.
- The on-chip output amplifiers allow rail-to-rail output swing, and the 3-wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range. Competitive devices are limited to 25-MHz clock rates at supply voltages in the 2.7-V to 3.6-V range. The serial interface is compatible with standard SPI™, QSPI, MICROWIRE, and DSP interfaces.
- The uDAC8x08/10/12 also offers daisy-chain operation, where an unlimited number of uDAC8x08/10/12s can be updated simultaneously using a single serial interface.
- There are two references for the uDAC8x08/10/12. One reference input serves channels A through D, while the other reference serves channels E through H. Each reference can be set independently between 0.5 V and VA, providing the widest possible output dynamic range.
- The uDAC8x08/10/12 is packaged in a 16-lead WQFN package and a 16-lead TSSOP package. The WQFN package makes the uDAC8x08/10/12 the smallest OCTAL DAC in its class.

## 2. Application

- Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources
- Programmable Attenuators
- Voltage Reference for ADCs
- Sensor Supply Voltage
- Range Detectors

## 3. Features

- Ensured Monotonicity
- Low Power Operation
- Rail-to-Rail Voltage Output
- Daisy-Chain Capability
- Power-on Reset to 0 V
- Simultaneous Output Updating
- Individual Channel Power-Down Capability
- Wide Power Supply Range (2.7 V to 5.5 V)
- Dual Reference Voltages With Range of 0.5 V to VA
- uDAC8X08 key features
  - Resolution 8 Bits
  - INL ±0.5 LSB (Maximum)
  - DNL 0.15 / –0.1 LSB (Maximum)
  - Settling Time 4.5 µs (Maximum)
- uDAC8X10 key features
  - Resolution 10 Bits
  - INL ±2 LSB (Maximum)
  - DNL 0.35 / –0.2 LSB (Maximum)
  - Settling Time 6 µs (Maximum)
- uDAC8X12 key features
  - Resolution 12 Bits
  - INL ±8 LSB (Maximum)
  - DNL 0.75 / –0.4 LSB (Maximum)
  - Settling Time 8.5 µs (Maximum)
- Zero Code Error 15 mV (Maximum)
- Full-Scale Error –0.75 %FSR (Maximum)
- Supply Power
  - 1.95 mW (3 V) / 4.85 mW (5 V) Typical
  - Power Down 0.3 µW (3 V) / 1 µW (5 V) Typical
- Operating Temperature Range of –40°C to 125°C
- 3mmx3mm QFN Smallest Package in the Industry

## 4. Device information

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| uDAC8x08<br>uDAC8x10<br>uDAC8x12 | TSSOP (16) | 5.0 mm × 4.4 mm |
| | WQFN (16) | 3.0 mm × 3.0 mm |

## 5. Simplified Schematic

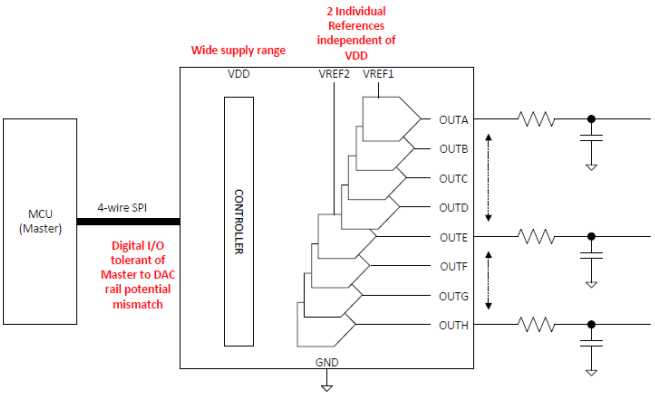



Figure 1. Simplified Schematic

## 1. Description (continued)

- The uDAC8x08/10/12 has a 16-bit input shift register that controls the mode of operation, the power-down condition, and the register/output value of the DAC channels. All eight DAC outputs can be updated simultaneously or individually.
- The power-down feature of the uDAC8x08/10/12 allows each DAC to be independently powered with three different termination options. With all the DAC channels powered down, power consumption reduces to less than 0.3 µW at 3 V and less than 1 µW at 5 V. The low power consumption and small packages of the uDAC8x08/10/12 make it an excellent choice for use in battery-operated equipment.
- The uDAC8x08/10/12 operates over the extended industrial temperature range of –40°C to 125°C.

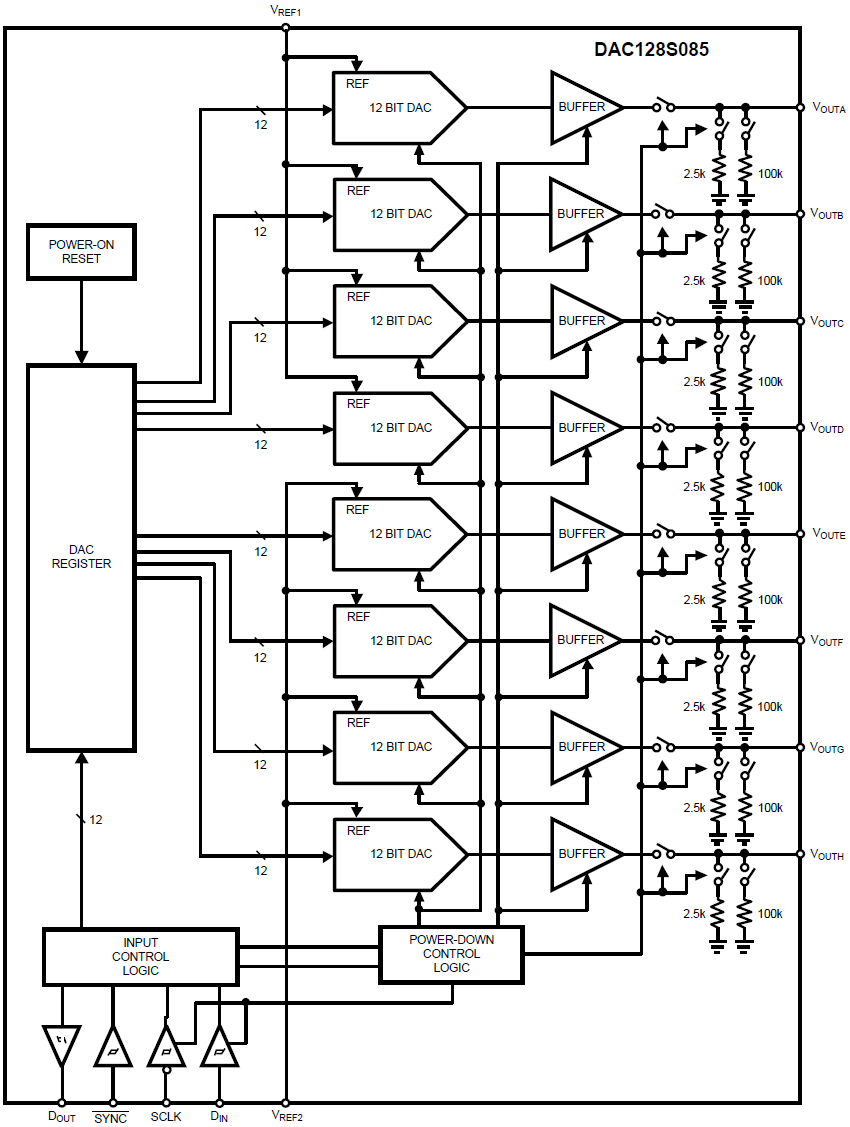



Figure 2. Diagram Block

CATALOG

## 6. Pin Configuration and Functions

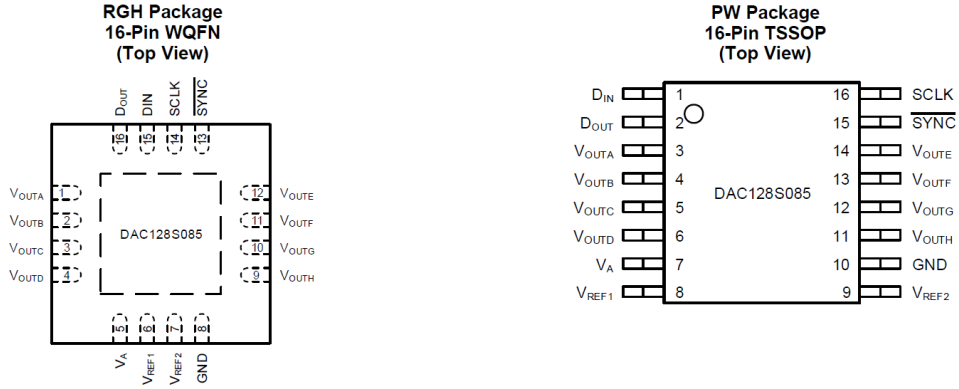



Figure 3. Pin configuration and functions

### Pin Functions

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | TSSOP NO. | WQFN NO. | | |
| $D_{IN}$ | 1 | 15 | Digital Input | Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of SYNC. |
| $D_{OUT}$ | 2 | 16 | Digital Output | Serial Data Output. $D_{OUT}$ is utilized in daisy chain operation and is connected directly to a $D_{IN}$ pin on another uDAC8x08/10/12. Data is not available at $D_{OUT}$ unless SYNC remains low for more than 16 SCLK cycles. |
| GND | 10 | 8 | Ground | Ground reference for all on-chip circuitry. |
| SCLK | 16 | 14 | Digital Input | Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin. |
| $\overline{SYNC}$ | 15 | 13 | Digital Input | Frame Synchronization Input. When this pin goes low, data is written into the DAC's input shift register on the falling edges of SCLK. After the 16th falling edge of SCLK, a rising edge of SYNC causes the DAC to be updated. If SYNC is brought high before the 15th falling edge of SCLK, the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC. |
| $V_A$ | 7 | 5 | Supply | Power supply input. Must be decoupled to GND. |
| $V_{OUTA}$ | 3 | 1 | Analog Output | Channel A Analog Output Voltage. |
| $V_{OUTB}$ | 4 | 2 | Analog Output | Channel B Analog Output Voltage. |
| $V_{OUTC}$ | 5 | 3 | Analog Output | Channel C Analog Output Voltage. |
| $V_{OUTD}$ | 6 | 4 | Analog Output | Channel D Analog Output Voltage. |
| $V_{OUTE}$ | 14 | 12 | Analog Output | Channel E Analog Output Voltage. |
| $V_{OUTF}$ | 13 | 11 | Analog Output | Channel F Analog Output Voltage. |
| $V_{OUTG}$ | 12 | 10 | Analog Output | Channel G Analog Output Voltage. |
| $V_{OUTH}$ | 11 | 9 | Analog Output | Channel H Analog Output Voltage. |
| $V_{REF1}$ | 8 | 6 | Analog Input | Unbuffered reference voltage shared by Channels A, B, C, and D. Must be decoupled to GND. |
| $V_{REF2}$ | 9 | 7 | Analog Input | Unbuffered reference voltage shared by Channels E, F, G, and H. Must be decoupled to GND. |
| PAD (WQFN only) | — | 17 | Ground | Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow. |

# 7. Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Voltage, $V_A$ | | 6.5 | V |
| Voltage on any Input Pin | −0.3 | 6.5 | V |
| Input Current at Any Pin (3) | | 10 | mA |
| Package Input Current(3) | | 30 | mA |
| Power Consumption at $T_A$ = 25°C | | See (4) | |
| Junction Temperature | | 150 | °C |
| Storage Temperature, $T_{stg}$ | −65 | 150 | °C |

## 7.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2500 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |
| | Machine Model | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Operating Temperature Range | −40 ≤ $T_A$ ≤ +125 | | °C |
| Supply Voltage, $V_A$ | 2.7 | 5.5 | V |
| Reference Voltage, $V_{REF1,2}$ | 0.5 | $V_A$ | V |
| Digital Input Voltage (1) | 0.0 | 5.5 | V |
| Output Load | 0 | 1500 | pF |
| SCLK Frequency | | 40 | MHz |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | uDAC8x08/10/12 PW (TSSOP) 16 PINS | uDAC8x08/10/12 RGH (WQFN) 16 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 98 | 34 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 31 | 25 | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 43 | 11 | |
| $\varphi_{JT}$ | Junction-to-top characterization parameter | 2 | 0.2 | |
| $\varphi_{JB}$ | Junction-to-board characterization parameter | 43 | 11 | |

## 7.5 Electrical Characteristics

The following specifications apply for $V_A$ = 2.7 V to 5.5 V, $V_{REF1}$ = $V_{REF2}$ = $V_A$, $C_L$ = 200 pF to GND, $f_{SCLK}$ = 30 MHz, input code range 48 to 4047. All limits are at $T_A$ = 25°C, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | |
| **uDAC8x08** | | | | | | |
| | Resolution | TMIN ≤ TA ≤ TMAX | 8 | | | Bits |
| | Monotonicity | TMIN ≤ TA ≤ TMAX | 8 | | | Bits |
| INL | Integral Non-Linearity | TMIN ≤ TA ≤ TMAX | | ±0.12 | ±0.5 | LSB |
| DNL | Differential Non-Linearity | TMIN ≤ TA ≤ TMAX | | 0.03 | 0.15 | LSB |
| | | TMIN ≤ TA ≤ TMAX | −0.1 | −0.02 | | LSB |
| **uDAC8x10** | | | | | | |
| | Resolution | TMIN ≤ TA ≤ TMAX | 10 | | | Bits |
| | Monotonicity | TMIN ≤ TA ≤ TMAX | 10 | | | Bits |
| INL | Integral Non-Linearity | TMIN ≤ TA ≤ TMAX | | ±0.5 | ±2 | LSB |
| DNL | Differential Non-Linearity | TMIN ≤ TA ≤ TMAX | | 0.08 | 0.35 | LSB |
| | | TMIN ≤ TA ≤ TMAX | −0.04 | −0.2 | | LSB |
| **uDAC8x12** | | | | | | |
| | Resolution | TMIN ≤ TA ≤ TMAX | 12 | | | Bits |
| | Monotonicity | TMIN ≤ TA ≤ TMAX | 12 | | | Bits |
| INL | Integral Non-Linearity | TMIN ≤ TA ≤ TMAX | | ±2 | ±8 | LSB |
| DNL | Differential Non-Linearity | TMIN ≤ TA ≤ TMAX | | 0.15 | 0.75 | LSB |
| | | TMIN ≤ TA ≤ TMAX | −0.4 | −0.09 | | LSB |
| ZE | Zero Code Error | $I_{OUT}$ = 0 | | 5 | 15 | mV |
| FSE | Full-Scale Error | $I_{OUT}$ = 0 | | −0.1 | −0.75 | %FSR |
| GE | Gain Error | | | −0.2 | −1 | %FSR |
| ZCED | Zero Code Error Drift | | | −20 | | µV/°C |
| TC GE | Gain Error Tempco | | | −1 | | ppm/°C |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output Voltage Range | | TMIN ≤ TA ≤ TMAX | 0 | | VREF1,2 | V |
| IOZ | High-Impedance Output Leakage Current | TMIN ≤ TA ≤ TMAX | | | ±1 | µA |
| ZCO | Zero Code Output | $V_A$ = 3 V, $I_{OUT}$ = 200 µA | | 10 | | mV |
| | | $V_A$ = 3 V, $I_{OUT}$ = 1 mA | | 45 | | mV |
| | | $V_A$ = 5 V, $I_{OUT}$ = 200 µA | | 8 | | mV |
| | | $V_A$ = 5 V, $I_{OUT}$ = 1 mA | | 34 | | mV |
| FSO | Full Scale Output | $V_A$ = 3 V, $I_{OUT}$ = 200 µA | | 2.984 | | V |
| | | $V_A$ = 3 V, $I_{OUT}$ = 1 mA | | 2.933 | | V |
| | | $V_A$ = 5 V, $I_{OUT}$ = 200 µA | | 4.987 | | V |
| | | $V_A$ = 5 V, $I_{OUT}$ = 1 mA | | 4.955 | | V |

## 7.5 Electrical Characteristics

The following specifications apply for $V_A$ = 2.7 V to 5.5 V, $V_{REF1}$ = $V_{REF2}$ = $V_A$, $C_L$ = 200 pF to GND, $f_{SCLK}$ = 30 MHz, input code range 48 to 4047. All limits are at $T_A$ = 25°C, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| IOS | Output Short Circuit Current (source) | $V_A$ = 3 V, $V_{OUT}$ = 0 V, Input Code = FFFh | | | −50 | | mA |
| | | $V_A$ = 5 V, $V_{OUT}$ = 0 V, Input Code = FFFh | | | −60 | | mA |
| IOS | Output Short Circuit Current (sink) | $V_A$ = 3 V, $V_{OUT}$ = 3 V, Input Code = 000h | | | 50 | | mA |
| | | $V_A$ = 5 V, $V_{OUT}$ = 5 V, Input Code = 000h | | | 70 | | mA |
| $I_O$ | Continuous Output Current per channel | $T_A$ = 105°C | | | | 10 | mA |
| | | $T_A$ = 125°C | | | | 6.5 | mA |
| $C_L$ | Maximum Load Capacitance | $R_L$ = ∞ | | | 1500 | | pF |
| | | $R_L$ = 2 kΩ | | | 1500 | | pF |
| ZOUT | DC Output Impedance | | | | 8 | | Ω |
| **REFERENCE INPUT CHARACTERISTICS** | | | | | | | |
| $V_{REF1,2}$ | Input Range Minimum | | | | 0.5 | | V |
| | | TMIN ≤ TA ≤ TMAX | | 2.7 | | $V_A$ | |
| | Input Impedance | | | | 30 | | kΩ |
| **LOGIC INPUT CHARACTERISTICS** | | | | | | | |
| $I_{IN}$ Input Current | | TMIN ≤ TA ≤ TMAX | | | | ±1 | µA |
| VIL | Input Low Voltage | $V_A$ = 2.7 V to 3.6 V | | | 1 | 0.6 | V |
| | | $V_A$ = 4.5 V to 5.5 V | | | 1.1 | 0.8 | V |
| VIH | Input High Voltage | $V_A$ = 2.7 V to 3.6 V | | 2.1 | 1.4 | | V |
| | | $V_A$ = 4.5 V to 5.5 V | | 2.4 | 2 | | V |
| CIN | Input Capacitance | TMIN ≤ TA ≤ TMAX | | | | 3 | pF |
| **POWER REQUIREMENTS** | | | | | | | |
| $V_A$ | Supply Voltage Minimum | TMIN ≤ TA ≤ TMAX | | 2.7 | | 5.5 | V |
| $I_N$ | Normal Supply Current for supply pin $V_A$ | $f_{SCLK}$ = 30 MHz, output unloaded | $V_A$ = 2.7 V to 3.6 V | | 460 | 560 | µA |
| | | | $V_A$ = 4.5 V to 5.5 V | | 650 | 830 | µA |
| | Normal Supply Current for VREF1 or VREF2 | $f_{SCLK}$ = 30 MHz, output unloaded | $V_A$ = 2.7 V to 3.6 V | | 95 | 130 | µA |
| | | | $V_A$ = 4.5 V to 5.5 V | | 160 | 220 | µA |
| $I_{ST}$ | Static Supply Current for supply pin $V_A$ | $f_{SCLK}$ = 0, output unloaded | $V_A$ = 2.7 V to 3.6 V | | 370 | | µA |
| | | | $V_A$ = 4.5 V to 5.5 V | | 440 | | µA |
| | Static Supply Current for VREF1 or VREF2 | $f_{SCLK}$ = 0, output unloaded | $V_A$ = 2.7 V to 3.6 V | | 95 | | µA |
| | | | $V_A$ = 4.5 V to 5.5 V | | 160 | | µA |
| $I_{PD}$ | Total Power Down Supply Current for all PD Modes | $f_{SCLK}$ = 30 MHz, SYNC = $V_A$ and $D_{IN}$ = 0V after PD mode loaded | $V_A$ = 2.7 V to 3.6 V | | 0.2 | 1.5 | µA |
| | | | $V_A$ = 4.5 V to 5.5 V | | 0.5 | 3 | µA |
| | | $f_{SCLK}$ = 0, SYNC = $V_A$ and $D_{IN}$ = 0V after PD mode loaded | $V_A$ = 2.7 V to 3.6 V | | 0.1 | 1 | µA |
| | | | $V_A$ = 4.5 V to 5.5 V | | 0.2 | 2 | µA |
| $P_N$ | Total Power Consumption (output unloaded) | $f_{SCLK}$ = 30 MHz, output unloaded | $V_A$ = 2.7 V to 3.6 V | | 1.95 | 3 | mW |
| | | | $V_A$ = 4.5 V to 5.5 V | | 4.85 | 7 | mW |
| | | $f_{SCLK}$ = 0, output unloaded | $V_A$ = 2.7 V to 3.6 V | | 1.68 | | mW |
| | | | $V_A$ = 4.5 V to 5.5 V | | 3.8 | | mW |
| $P_{PD}$ | Total Power Consumption in PPD all PD Modes, | $f_{SCLK}$ = 30 MHz, SYNC = $V_A$ and $D_{IN}$ = 0V after PD mode loaded | $V_A$ = 2.7 V to 3.6 V | | 0.6 | 5.4 | µW |
| | | | $V_A$ = 4.5 V to 5.5 V | | 2.5 | 16.5 | µW |
| | | $f_{SCLK}$ = 0, SYNC = $V_A$ and $D_{IN}$ = 0V after PD mode loaded | $V_A$ = 2.7 V to 3.6 V | | 0.3 | 3.6 | µW |
| | | | $V_A$ = 4.5 V to 5.5 V | | 1 | 11 | µW |

## 7.6 AC and Timing Characteristics

The following specifications apply for VA = 2.7 V to 5.5 V, VREF1,2 = VA, CL = 200 pF to GND, fSCLK = 30 MHz, input code range 48 to 4047. All limits are at TA = 25°C, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK Frequency | | | | 40 | | MHz |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | | | 30 | MHz |
| $t_s$ | Output Voltage Settling Time | **uDAC8x08** | 40h to C0h code change $R_L$ = 2 kΩ, $C_L$ = 200 pF | | 3 | 4.5 | µs |
| | | **uDAC8x10** | 100h to 300h code change $R_L$ = 2 kΩ, $C_L$ = 200 pF | | 4.5 | 6 | µs |
| | | **uDAC8x12** | 400h to C00h code change $R_L$ = 2 kΩ, $C_L$ = 200 pF | | 6 | 8.5 | µs |
| SR | Output Slew Rate | | | | 1 | | V/µs |
| GI | Glitch Impulse | **uDAC8x08** Code change from 80h to 7Fh;<br>**uDAC8x10** Code change from 200h to 1FFh;<br>**uDAC8x12** Code change from 800h to 7FFh; | | | 40 | | nV-sec |
| DF | Digital Feedthrough | | | | 0.5 | | nV-sec |
| DC | Digital Crosstalk | | | | 0.5 | | nV-sec |
| CROSS | DAC-to-DAC Crosstalk | | | | 1 | | nV-sec |
| MBW | Multiplying Bandwidth | $V_{REF1,2}$ = 2.5 V ± 2 Vpp | | | 360 | | kHz |
| THD+N | Total Harmonic Distortion Plus Noise | $V_{REF1,2}$ = 2.5 V ± 0.5 Vpp 100 Hz < $f_{IN}$ < 20 kHz | | | −80 | | dB |
| ONSD | Output Noise Spectral Density | **uDAC8x08** DAC Code = 80 h, 10 kHz<br>**uDAC8x10** DAC Code = 200 h, 10 kHz<br>**uDAC8x12** DAC Code = 800 h, 10 kHz | | | 40 | | nV/√(Hz) |
| ON | Output Noise | BW = 30 kHz | | | 14 | | µV |
| $t_{WU}$ | Wake-Up Time | $V_A$ = 3 V | | | 3 | | µs |
| | | $V_A$ = 5 V | | | 20 | | µs |
| 1/$f_{SCLK}$ | SCLK Cycle Time. | | | | 25 | | ns |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | 33 | | | ns |
| $t_{CH}$ | SCLK High time. | | | 7 | 7 | | ns |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | 10 | | | ns |
| $t_{CL}$ | SCLK Low Time. | | | 7 | 7 | | ns |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | 10 | | | ns |
| $t_{SS}$ | SYNC Set-up Time prior to SCLK Falling Edge. | | | | 3 | 1 / $f_{SCLK}$ - 3 | ns |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | 10 | | | ns |
| $t_{DS}$ | Data Set-Up Time prior to SCLK Falling Edge. | | | | 1 | | ns |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | 2.5 | | | ns |
| $t_{DH}$ | Data Hold Time after SCLK Falling Edge. | | | | 1 | | ns |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | 2.5 | | | ns |
| $t_{SH}$ | SYNC Hold Time after the 16th falling edge of SCLK. | | | | 0 | 1 / $f_{SCLK}$ - 3 | ns |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | 3 | | | ns |
| $t_{SYNC}$ | SYNC High Time. | | | | 5 | | ns |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | 15 | | | ns |

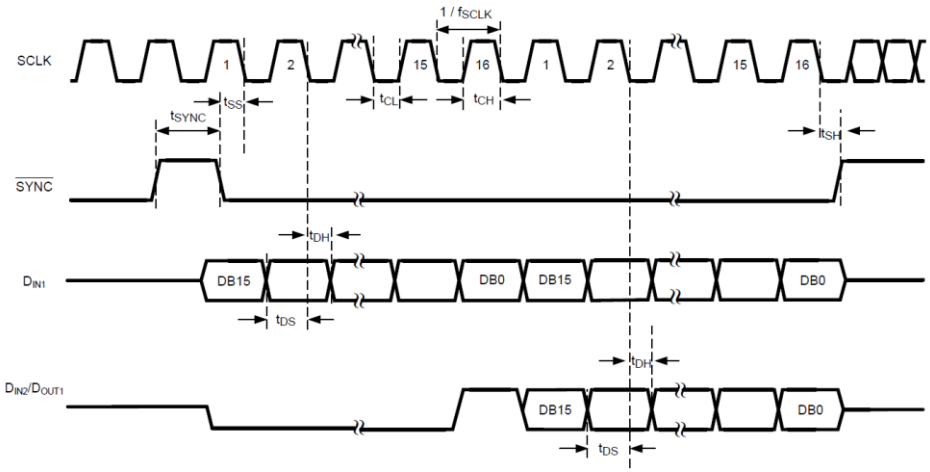



Figure 4. Serial Timing Diagram

## 8. Typical Characteristics

$V_A$ = 2.7 V to 5.5 V, $V_{REF1,2}$ = $V_A$, $f_{SCLK}$ = 30 MHz, $T_A$ = 25°C, unless otherwise stated

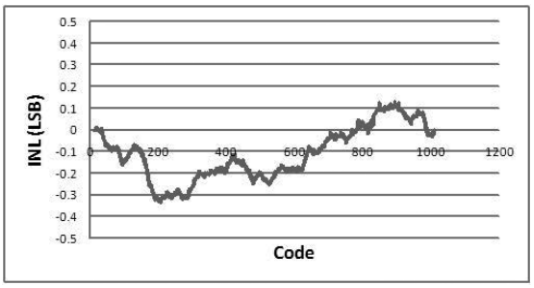



Figure 5. uDAC8x10 typical INL

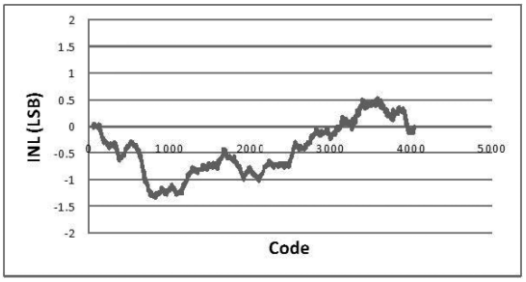



Figure 6. uDAC8x12 typical INL

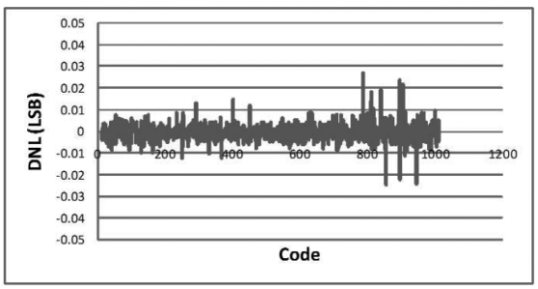



Figure 7. uDAC8x10 typical DNL

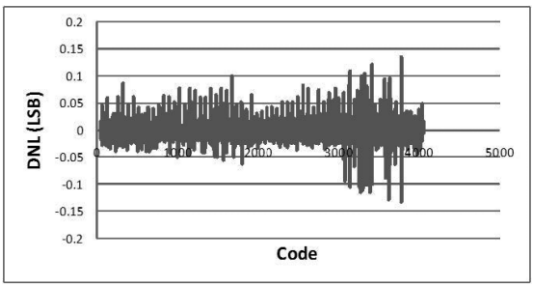



Figure 8. uDAC8x12 typical DNL

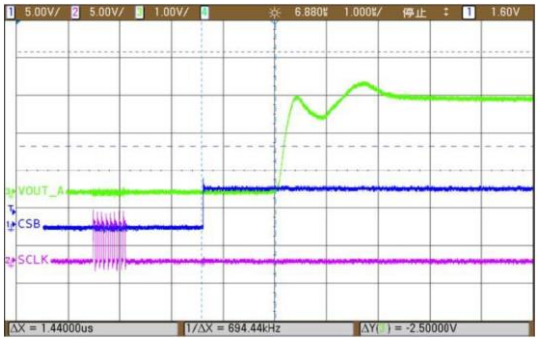



Figure 9. DAC Wake-up process

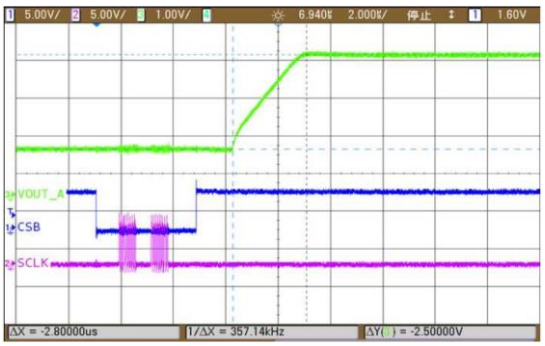



Figure 10. Output setting process (25%FSR to 75%FSR)

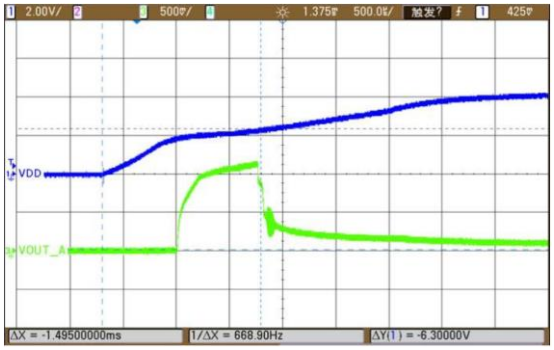



Figure 11. Power-On Reset

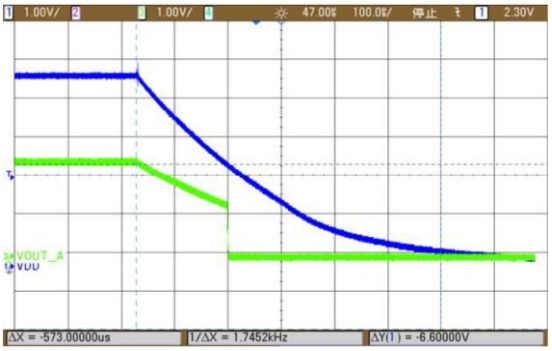



Figure 12. Power Down

## 9. Detailed Description

### 9.1 Overview

The uDAC8x08/10/12 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer.

The output amplifiers are rail-to-rail, providing an output voltage range of 0 V to VA when the reference is VA. The output amplifiers are capable of driving a load of 2 kΩ in parallel with 1500 pF to ground or to VA.

The uDAC8x08/10/12 uses dual external references, VREF1 and VREF2, that are shared by channels A, B, C, D and channels E, F, G, H respectively. The reference pins are not buffered and have an input impedance of 30 kΩ.

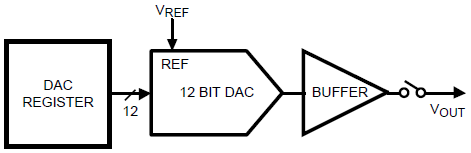



Figure 13. Single-Channel Block Diagram

### 9.2 DAC Architecture

The uDAC8x08/10/12 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer. The reference voltages are externally applied at VREF1 for DAC channels A through D and VREF2 for DAC channels E through H.

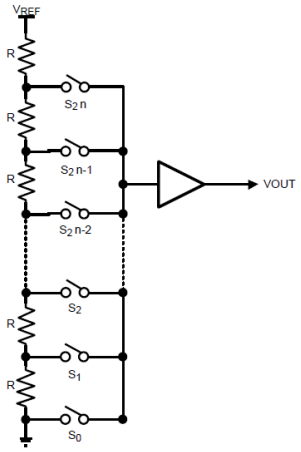



Figure 14. DAC Resistor String

The transfer function is like this:

$$V_{OUTA,B,C,D} = V_{REF1} \times (CODE / 2^N)$$

$$V_{OUTE,F,G,H} = V_{REF2} \times (CODE / 2^N)$$

### 9.3 Device Functional Modes

#### 9.3.1 Power-On Reset

The power-on reset circuit controls the output voltages of the eight DACs during power up. Upon application of power, the DAC registers are filled with zeros and the output voltages are set to 0 V. The outputs remain at 0 V until a valid write sequence is made.

#### 9.3.2 Power-Down Modes

The uDAC8x08/10/12 has three power-down modes where different output terminations can be selected (see Table 1). With all channels powered down, the supply current drops to 0.1 μA at 3 V and 0.2 μA at 5 V. By selecting the channels to be powered down in DB[7:0] with a 1, individual channels can be powered down separately or multiple channels can be powered down simultaneously. The three different

output terminations include high output impedance, 100 kΩ to GND, and 2.5 kΩ to GND.

The output amplifiers, resistor strings, and other linear circuitry are all shut down in any of the power-down modes. The bias generator, however, is only shut down if all the channels are placed in power down mode. The contents of the DAC registers are unaffected when in power down. Therefore, each DAC register maintains its value before the uDAC8x08/10/12 being powered down unless it is changed during the write sequence which instructed it to recover from power down. Minimum power consumption is achieved in the power-down mode with SYNC idled high, DIN idled low, and SCLK disabled.

Table 1. Power-Down Modes

| DB[15:12] | DB[11:8] | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OUTPUT IMPEDANCE |
|---|---|---|---|---|---|---|---|---|---|---|
| 1101 | XXXX | H | G | F | E | D | C | B | A | High-Z outputs |
| 1110 | XXXX | H | G | F | E | D | C | B | A | 100-kΩ outputs |
| 1111 | XXXX | H | G | F | E | D | C | B | A | 2.5-kΩ outputs |

## 9.4 Programming

### 9.4.1 Serial Interface

The three-wire interface is compatible with SPI, QSPI, and MICROWIRE, as well as most DSPs and operates at clock rates up to 40MHz. A valid serial frame contains 16 falling edges of SCLK.

A write sequence begins by bringing the SYNC line low. Once SYNC is low, the data on the DIN line is clocked into the 16-bit serial input register on the falling edges of SCLK. To avoid mis-clocking data into the shift register, it is critical that SYNC not be brought low on a falling edge of SCLK (see minimum and maximum setup times for SYNC in Figure 4 and Figure 15). On the 16th falling edge of SCLK, the last data bit is clocked into the register. The write sequence is concluded by bringing the SYNC line high. Once SYNC is high, the programmed function (a change in the DAC channel address, mode of operation or register contents) is executed. To avoid mis- clocking data into the shift register, it is critical that SYNC be brought high between the 16th and 17th falling edges of SCLK (see minimum and maximum hold times for SYNC in Figure 4 and Figure 15).

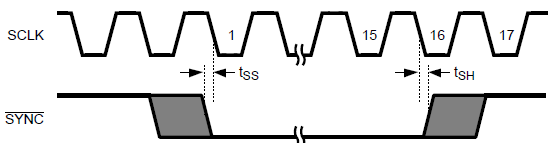



Figure 15. CS Setup and Hold Times

If SYNC is brought high before the 15th falling edge of SCLK, the write sequence is aborted and the data that has been shifted into the input register is discarded. If SYNC is held low beyond the 17th falling edge of SCLK, the serial data presented at DIN begins to be output on DOUT. More information on this mode of operation can be found in Daisy Chain Operation. In either case, SYNC must be brought high for the minimum specified time before the next write sequence is initiated with a falling edge of SYNC.Because the DIN buffer draws more current when it is high, it must be idled low between write sequences to minimize power consumption. On the other hand, SYNC must be idled high to avoid the activation of daisy chain operation where DOUT is active.

### 9.4.2 Daisy Chain Operation

Daisy chain operation allows communication with any number of uDAC8x08/10/12s using a single serial interface. As long as the correct number of data bits are input in a write sequence (multiple of sixteen bits), a rising edge of SYNC properly updates all DACs in the system.

To support multiple devices in a daisy chain configuration, SCLK and SYNC are shared across all uDAC8x08/10/12s and DOUT of the first DAC in the chain is connected to DIN of the second. Figure 30 shows three uDAC8x08/10/12s connected in daisy chain fashion. Similar to a single-channel write sequence, the conversion for a daisy chain operation begins on a falling edge of SYNC and ends on a rising edge of SYNC. A valid write sequence for n devices in a chain requires n times 16 falling edges to shift the entire input data stream through the chain. Daisy chain operation is specified for a maximum SCLK speed of 30MHz.

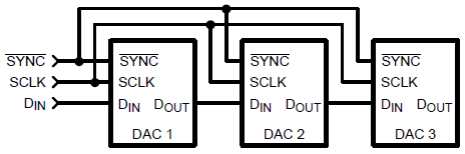



Figure 16. Daisy-Chain Configuration

The serial data output pin, DOUT, is available on the uDAC8x08/10/12 to allow daisy-chaining of multiple uDAC8x08/10/12 devices in a system. In a write sequence, DOUT remains low for the first fourteen falling edges of SCLK before going high on the fifteenth falling edge. Subsequently, the next sixteen falling edges of SCLK outputs the first sixteen data bits entered into DIN. Figure 17 shows the timing of three uDAC8x08/10/12s in Figure 16. In this instance, It takes forty-eight falling edges of SCLK followed by a rising edge of SYNC to load all three uDAC8x08/10/12s with the appropriate register data. On the rising edge of SYNC, the programmed function is executed in each uDAC8x08/10/12

simultaneously.

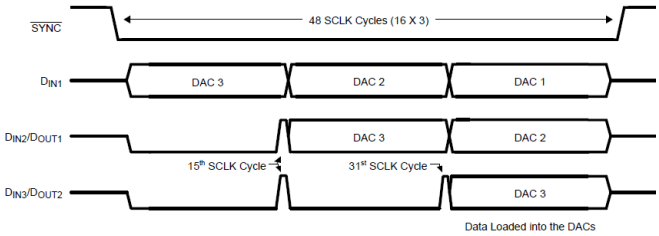



Figure 17. Daisy Chain Timing Diagram

## 9.5 Serial Input Register

The uDAC8x08/10/12 has four register function operation. DB[15:12] are command bits. DB[11:0] are data bits. For uDAC8x10, DB[1:0] is not available. For uDAC8x08, DB[3:0] is not available. For Detailed description, see register map Table 2.

Table 2. Register Map

| REGISTER FUNCTION | DB[15:12] | DB[11:0] | DESCRIPTION OF MODE |
|---|---|---|---|
| Commands Impacted by WRM and WTM | 0 0 0 0 | D11 D10 ... D3 D2 D1 D0 | WRM: D[11:0] written to ChA's data register only<br>WTM: ChA's output is updated by data in D[11:0] |
| | 0 0 0 1 | D11 D10 ... D3 D2 D1 D0 | WRM: D[11:0] written to ChB's data register only<br>WTM: ChB's output is updated by data in D[11:0] |
| | 0 0 1 0 | D11 D10 ... D3 D2 D1 D0 | WRM: D[11:0] written to ChC's data register only<br>WTM: ChC's output is updated by data in D[11:0] |
| | 0 0 1 1 | D11 D10 ... D3 D2 D1 D0 | WRM: D[11:0] written to ChD's data register only<br>WTM: ChD's output is updated by data in D[11:0] |
| | 0 1 0 0 | D11 D10 ... D3 D2 D1 D0 | WRM: D[11:0] written to ChE's data register only<br>WTM: ChE's output is updated by data in D[11:0] |
| | 0 1 0 1 | D11 D10 ... D3 D2 D1 D0 | WRM: D[11:0] written to ChF's data register only<br>WTM: ChF's output is updated by data in D[11:0] |
| | 0 1 1 0 | D11 D10 ... D3 D2 D1 D0 | WRM: D[11:0] written to ChG's data register only<br>WTM: ChG's output is updated by data in D[11:0] |
| | 0 1 1 1 | D11 D10 ... D3 D2 D1 D0 | WRM: D[11:0] written to ChH's data register only<br>WTM: ChH's output is updated by data in D[11:0] |
| Write Register and Write Through Modes | 1 0 0 0 | X X ... X X X X | WRM: The registers of each DAC Channel can be written to without causing their outputs to change. |
| | 1 0 0 1 | X X ... X X X X | WTM: Writing data to a channel's register causes the DAC output to change. |
| Special Command Operations | 1 0 1 0 | X X X X H G F E D C B A | Update Select: The DAC outputs of the channels selected with a 1 in DB[7:0] are updated simultaneously to the values in their respective control registers. |
| | 1 0 1 1 | D11 D10 ... D3 D2 D1 D0 | Channel A Write: the control register of Channel A and DAC output are updated to the data in DB[11:0]. The outputs of the other seven channels are also updated according to their respective control register values. |
| | 1 1 0 0 | D11 D10 ... D3 D2 D1 D0 | Broadcast: The data in DB[11:0] is written to all channels' control register and DAC output simultaneously. |
| Power Down Mode | 1 1 0 1 | X X X X H G F E D C B A | Output Impedance High-Z outputs |
| | 1 1 1 0 | X X X X H G F E D C B A | Output Impedance 100-kΩ outputs |
| | 1 1 1 1 | X X X X H G F E D C B A | Output Impedance 2.5-kΩ outputs |

### 9.5.1 Write Register and Write Through Modes

The uDAC8x08/10/12 has two modes of operation plus a few special command operations. The two modes of operation are Write Register Mode (WRM) and Write Through Mode (WTM). The mode of operation is controlled by the first four bits of the control register, DB15 through DB12. See Table 3 for a detailed summary.

Table 3. WRM and WTM Modes

| DB[15:12] | DB[11:0] | DESCRIPTION OF MODE |
|---|---|---|
| 1 0 0 0 | X ... X | WRM: The registers of each DAC Channel can be written to without causing their outputs to change. |
| 1 0 0 1 | X ...X | WTM: Writing data to a channel's register causes the DAC output to change. |

### 9.5.2 Commands Impacted by WRM and WTM

When the uDAC8x08/10/12 first powers up, the DAC is in WRM. In WRM, the registers of each individual DAC channel can be written to without causing the DAC outputs to be updated. This is accomplished by setting DB15 to 0, specifying the DAC register to be written to in DB[14:12], and entering the new DAC register setting in DB[11:0] (see Table 4).

The uDAC8x08/10/12 remains in WRM until the mode of operation is changed to WTM. The mode of operation is changed from WRM to WTM by setting DB[15:12] to 1001. Once in WTM, writing data to a DAC channel's register causes the DAC's output to be updated as well. Changing a DAC channel's register in WTM is accomplished in the same manner as it is done in WRM. However, in WTM the DAC's register and output are updated at the completion of the command (see Table 4). Similarly, the uDAC8x08/10/12 remains in WTM until the mode of operation is changed to WRM by setting DB[15:12] to 1000.

Table 4. Commands Impacted by WRM and WTM

| DB15 | DB[14:12] | DB[11:0] | Description of Mode |
|---|---|---|---|
| 0 | 0 0 0 | D11 D10 ... D1 D0 | WRM: D[11:0] written to ChA's data register only<br>WTM: ChA's output is updated by data in D[11:0] |
| 0 | 0 0 1 | D11 D10 ... D1 D0 | WRM: D[11:0] written to ChB's data register only<br>WTM: ChB's output is updated by data in D[11:0] |
| 0 | 0 1 0 | D11 D10 ... D1 D0 | WRM: D[11:0] written to ChC's data register only<br>WTM: ChC's output is updated by data in D[11:0] |
| 0 | 0 1 1 | D11 D10 ... D1 D0 | WRM: D[11:0] written to ChD's data register only<br>WTM: ChD's output is updated by data in D[11:0] |
| 0 | 1 0 0 | D11 D10 ... D1 D0 | WRM: D[11:0] written to ChE's data register only<br>WTM: ChE's output is updated by data in D[11:0] |
| 0 | 1 0 1 | D11 D10 ... D1 D0 | WRM: D[11:0] written to ChF's data register only<br>WTM: ChF's output is updated by data in D[11:0] |
| 0 | 1 1 0 | D11 D10 ... D1 D0 | WRM: D[11:0] written to ChG's data register only<br>WTM: ChG's output is updated by data in D[11:0] |
| 0 | 1 1 1 | D11 D10 ... D1 D0 | WRM: D[11:0] written to ChH's data register only<br>WTM: ChH's output is updated by data in D[11:0] |

### 9.5.3 Special Command Operations

As mentioned previously, the special command operations can be exercised at any time regardless of the mode of operation. There are three special command operations. The first command is exercised by setting data bits DB[15:12] to 1010. This allows a user to update multiple DAC outputs simultaneously to the values currently loaded in their respective control registers. This command is valuable if the user wants each DAC output to be at a different output voltage but still have all the DAC outputs change to their appropriate values simultaneously (see Table 5).

The second special command allows the user to alter the DAC output of channel A with a single write frame. This command is exercised by setting data bits DB[15:12] to 1011 and data bits DB[11:0] to the desired control register value. It also has the added benefit of causing the DAC outputs of the other channels to update to their current control register values as well. A user may choose to exercise this command to save a write sequence. For example, the user may wish to update several DAC outputs simultaneously, including channel A. To accomplish this task in the minimum number of write frames, the user would alter the control register values of all the DAC channels except channel A while operating in WRM. The last write frame would be used to exercise the special command Channel A Write Mode. In addition to updating channel A's control register and output to a new value, all of the other channels would be updated as well. At the end of this sequence of write frames, the uDAC8x08/10/12 would still be operating in WRM (see Table 5).

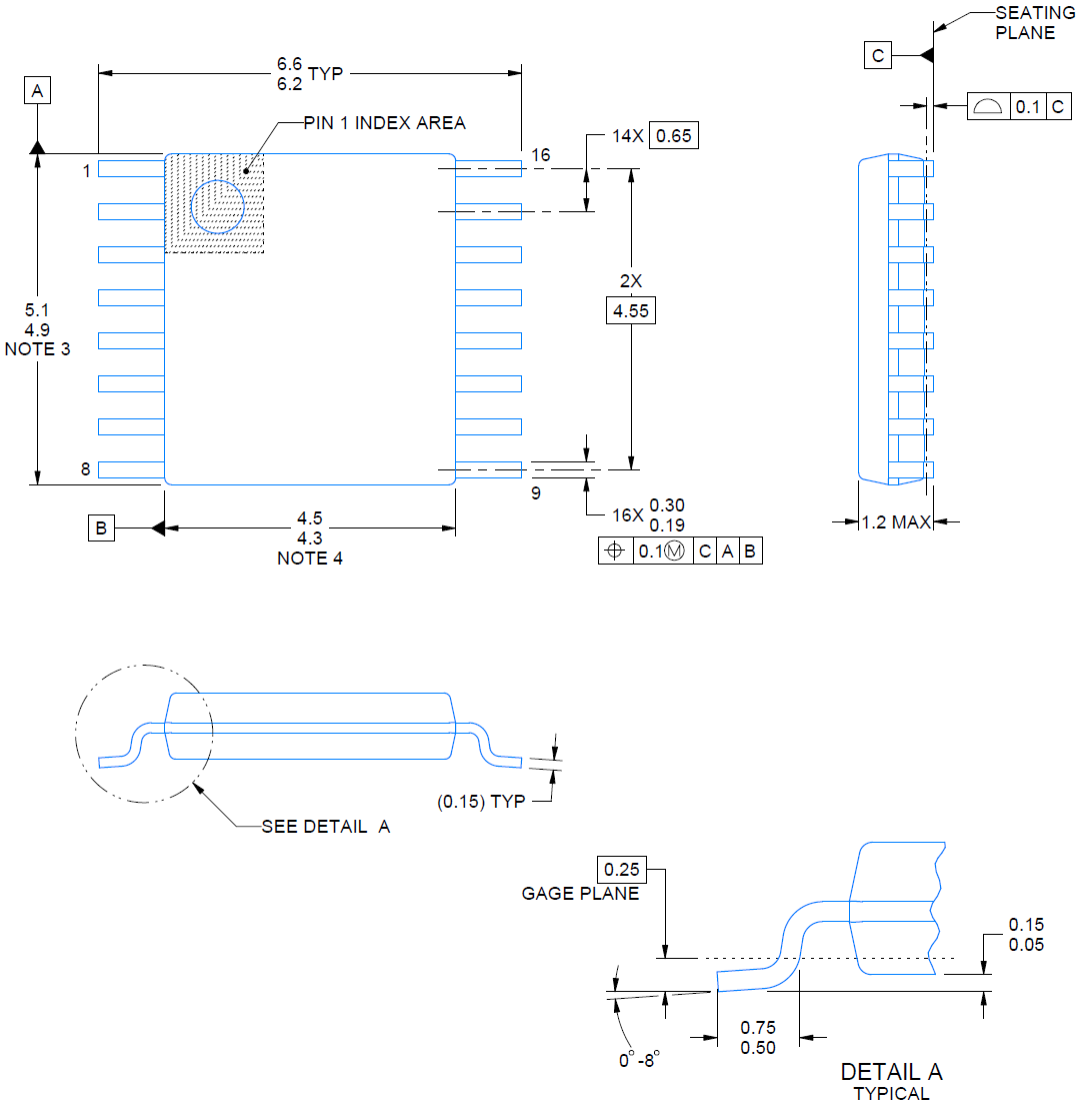
Table 5. Special Command Operations

| DB[15:12] | DB[11:0] | DESCRIPTION OF MODE |
|---|---|---|
| 1 0 1 0 | X X X X H G F E D C B A | Update Select: The DAC outputs of the channels selected with a 1 in DB[7:0] are updated simultaneously to the values in their respective control registers. |
| 1 0 1 1 | D11 D10 ... D3 D2 D1 D0 | Channel A Write: the control register of Channel A and DAC output are updated to the data in DB[11:0]. The outputs of the other seven channels are also updated according to their respective control register values. |
| 1 1 0 0 | D11 D10 ... D3 D2 D1 D0 | Broadcast: The data in DB[11:0] is written to all channels' control register and DAC output simultaneously. |

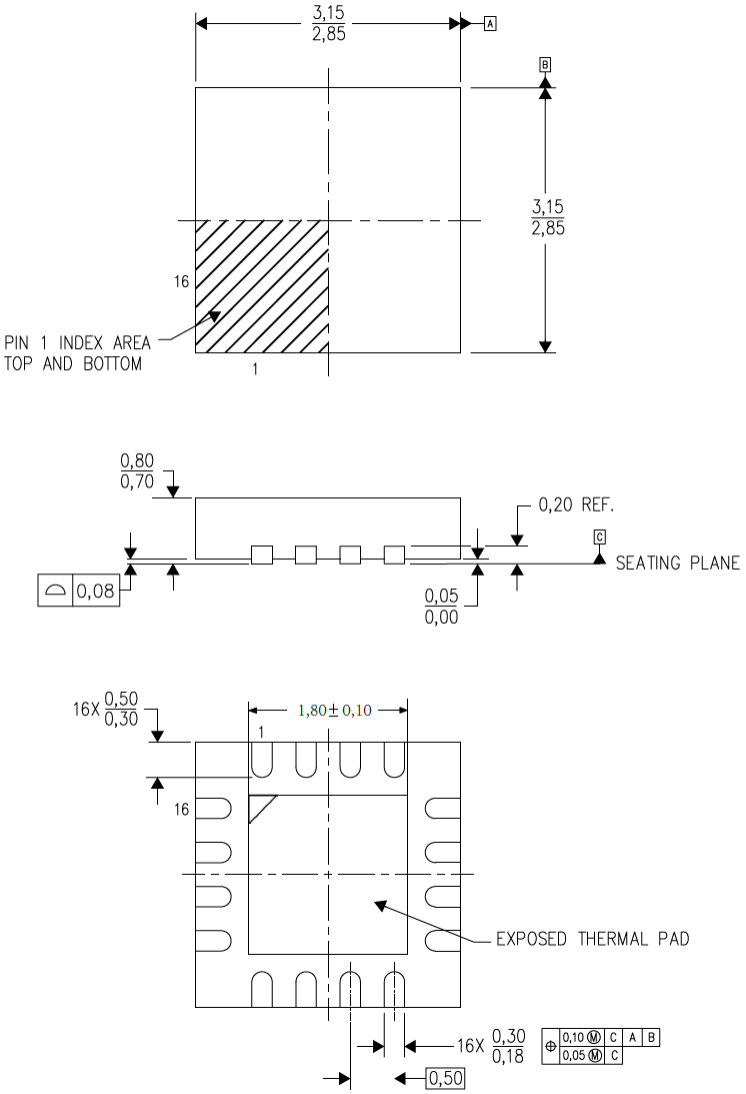
The third special command allows the user to set all the DAC control registers and outputs to the same level. This command is commonly referred to as broadcast mode because the same data bits are being broadcast to all of the channels simultaneously. This command is exercised by setting data bits DB[15:12] to 1100 and data bits DB[7:0] to the value that the user wishes to broadcast to all the DAC control registers. Once the command is exercised, each DAC output is updated by the new control register value. This command is frequently used to set all the DAC outputs to some known voltage such as 0 V, VREF / 2, or Full Scale. A summary of the commands can be found in Table 5.

## 10. PACKAGE OUTLINE

### 10.1 TSSOP PACKAGE



### 10.2 WQFN 3mmx3mm



## 11. Device Ordering Information

| PRODUCT | ORDERING NUMBER | TEMPRANGE | PACKAGE | PAKEAGE MARKING | TRANSPOT MEDIA,QUANTILY |
|---|---|---|---|---|---|
| **uDAC8x08** | uDAC8x08QF | -40℃~125℃ | QFN16 | 8X08Q | Reel,2500 |
| | uDAC8x08TS | -40℃~125℃ | TSSOP16 | 8X08 | Reel,2500 |
| **uDAC8x10** | uDAC8x10QF | -40℃~125℃ | QFN16 | 8X10Q | Reel,2500 |
| | uDAC8x10TS | -40℃~125℃ | TSSOP16 | 8X10 | Reel,2500 |
| **uDAC8x12** | uDAC8x12QF | -40℃~125℃ | QFN16 | 8X12Q | Reel,2500 |
| | uDAC8x12TS | -40℃~125℃ | TSSOP16 | 8X12 | Reel,2500 |